

AUG-03-2004(TUE) 11:24 GALLAGHER & LATHROP

(FAX) 415 989 0910

P. 001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED
CENTRAL FAX CENTER

Applicants: Masahiro Ishida, et al.

Examiner: Ayal I. Sharon

AUG 03 2004

Serial No.: 09/699,077

Art Unit: 2123

Filing Date: October 27, 2000

Title: Method and Apparatus for
Fault Simulation of
Semiconductor Integrated
Circuit

Conf. No. 9031

OFFICIAL

August 3, 2004
San Francisco, California

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

Sir:

This communication is submitted in response to the office action mailed May 3, 2004
(referred to herein as "Office Action").

BEST AVAILABLE COPY

- 1 -

Docket: KPO089

PAGE 1/6 * RCVD AT 8/3/2004 2:25:07 PM [Eastern Daylight Time] * SVR:USPTO-EXRF-1/0 * DNI:8729306 * CSID:415 989 0910 * DURATION (mm:ss):02:06